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EXAMINER	
SPITTLE, MATTHEW D	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 09/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/723,896	SHAW, RONALD D.	
	Examiner	Art Unit	
	Matthew D. Spittle	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/1/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 2, 5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bajikar in view of Rollig et al.

With regard to claim 1, Bajikar teaches an information system comprising:

components operable to process information (page 3, where components may be interpreted as CPU, RAM, trusted platform module, trusted mobile keyboard controller, memory controller hub);

a trusted bus operable to securely communicate information between the component (page 6 – 7, where trusted bus may be interpreted as trusted channel);

an integrated keyboard operable to accept user inputs (page 3, 6, where integrated keyboard may be interpreted as a key matrix scan);

an integrated pointing device operable to accept user inputs (integrated mobile pointing device/IPD; page 3, 16);

a microcontroller interfaced with the keyboard and pointing device, the microcontroller operable to convert keyboard and pointing device user inputs into HID packets and to embed the HID packets as messages on the trusted bus (page 10, 11, 15, 19);

HID trusted registers operable to provide the HID packets to one or more of the components (pages 8 – 11).

Bajikar fails to explicitly teach a motherboard, however, it would have been well-known to one of ordinary skill in the art at the time of invention by applicant to incorporate a motherboard to provide a means for mounting the said components and supporting the system buses.

Bajikar also fails to teach a state machine associated with the motherboard and interfaced with the trusted bus.

Rollig et al. teach a state machine interfaced with the trusted bus, the state machine operable to extract the HID packets from the trusted bus (paragraphs 73, 79, where trusted bus may be interpreted as an SMBus; claim 1, 4th paragraph). Rollig et al. fail to explicitly teach a motherboard, however, teach that the state machine may be integrated into a circuit chip (paragraph 73). It would have been well-known to one of

ordinary skill in the art at the time of invention by applicant to affix the said circuit chip onto a motherboard in order to mount it and provide it with connectivity to a bus.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to include the state machine of Rollig et al. in the information handling system of Bajikar in order to provide a means of extracting the HID packets from the trusted bus. This would have been obvious since Rollig et al. teach that a finite state machine can receive and interpret instructions and data, and transfer the data between a trusted bus and register set (paragraph 73, 79; claim 1, 4th paragraph).

With regard to claim 2, Rollig et al. teach the additional limitation wherein the trusted bus comprises an SMBus (paragraph 1, 2).

With regard to claim 5, Bajikar teaches the additional limitation of the information handling system of claim 1 further comprising:

An external controller interfaced with the motherboard, the external controller operable to accept user inputs from a external keyboard and to convert the external keyboard inputs into HID packets (page 16; where, controller is interpreted as being a microcontroller). Although Bajikar does not specifically teach an external keyboard, it would have been well known to one of ordinary skill in this art at the time of invention by applicant that an external keyboard can be connected to an external PS/2 port, which the Bajikar does teach, and is connected to the external controller.

HID non-trusted registers interfaced with the external controller and operable to provide the external keyboard input HID packets to one or more of the components (page 16, registers 60/64h and 62/66h; components are interpreted as RAM/ROM).

Examiner interprets HID packets as being any data packet produced by a human interface device, such as a keyboard.

With regard to claim 7, Bajikar teaches the additional limitation wherein the integrated pointing device comprises a touchpad (page 10).

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bajikar in view of Rollig et al., and further in view of Semtech.

Bajikar and Rollig et al. fail to teach the information handling system of Claim 1 wherein the trusted bus comprises an SPI bus.

Semtech teaches using an SPI bus as an interface for a keyboard and other input devices (page 2). Therefore, it would have been obvious to one or ordinary skill in this art at the time of invention by applicant to modify the information handling system of Bajikar and Rollig et al. to use the SPI bus as taught by Semtech. This would have been obvious since Semtech teaches that their products are designed for for HID functionality in information appliances (page 1).

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bajikar in view of Rollig et al., and further in view of Mueller.

Rollig et al. teach the additional limitation wherein the trusted bus comprises an SMBus (paragraph 1, 2), however Rollig et al. fail to teach a dual SMBus for bi-directional communication.

Mueller teaches that full-duplex transmission allows for simultaneous full bandwidth transmission in both directions along with reducing start-up and turnaround delays. It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to incorporate a dual SMBus to gain these advantages (column 1, lines 12 – 27).

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bajikar, in view of Rollig et al., and further in view of Walker.

Bajikar and Rollig et al. teach a chipset for communicating with external devices (page 6), but fail to teach the state machine comprising firmware associated with the chipset.

Walker teaches a state machine comprising firmware associated with a chipset, where microprogramming may be interpreted as firmware). It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to implement the state machine of Rollig et al. in firmware associated with the chipset. This would have been obvious since Walker teaches firmware-programmed state machines reduce the number of required components, are very regular, easier to modify when changes are needed, and reduce the complexity of the hardware (column 5, lines 37 – 46).

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bajikar in view of Bajikar et al.

Bajikar teaches a method for communicating user inputs to an information handling system, the method comprising:

Communicating the inputs to a common microcontroller (pages 14 – 16);

Converting the inputs with the microcontroller into HID packets (page 11, 19);

Bajikar fails to explicitly teach detecting user inputs at an integrated pointing device and an integrated keyboard. However, since he or she does teach the presence of these devices, examiner regards detecting user inputs at the said devices to be inherent in the system since the devices would not provide utility otherwise.

Bajikar fails to teach embedding the HID packets as messages on an internal motherboard bus, and extracting the HID packets at the motherboard for processing.

Bajikar et al. teach embedding the HID packets as messages on an internal motherboard bus (paragraph 9, 11, 17).

Bajikar et al. fail to explicitly teach extracting the HID packets at the motherboard for processing. However, Bajikar et al. teach a chipset coupled to the internal motherboard bus able to deliver data to and from the processor and memory. Examiner interprets this as meaning the chipset is able to extract the HID packets from the motherboard bus and deliver them to the CPU for processing (paragraph 9).

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bajikar in view of Bajikar et al., and further in view of Loh et al.

Bajikar and Bajikar et al. fail to teach the method of claim 8 wherein the internal motherboard bus comprises an I2C bus.

Loh et al. teach using an I2C bus to communicate between a keyboard controller that is linked with a keyboard and/or integrated pointing device and a processor (paragraph 10, 13, 15, claim 1, 2). Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to include the method of using an I2C bus as taught by Loh et al. in the method of Bajikar and Bajikar et al.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bajikar in view of Bajikar et al., and further in view of Semtech.

Bajikar and Bajikar et al. fail to teach the method of Claim 8 wherein the trusted bus comprises an SPI bus.

Semtech teaches using an SPI bus as an interface for a keyboard and other input devices (page 2). Therefore, it would have been obvious to one or ordinary skill in this art at the time of invention by applicant to modify the information handling system of Bajikar and Rollig et al. to use the SPI bus as taught by Semtech. This would have been obvious since Semtech teaches that their products are designed for HID functionality in information appliances (page 1).

Claims 9, 12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bajikar in view of Bajikar et al., in view of Loh et al., and further in view of Maxim/Dallas Semiconductor.

With regard to claim 9, Loh et al. teach embedding HID packets received from a keyboard controller onto an I2C bus as I2C messages (paragraphs 10, 13, 15). Loh et al. fail to explicitly describe a motherboard, however, examiner notes a motherboard would have been an inherent structure in the system of Loh et al. in order to provide a means of mounting and interconnecting components and buses. Loh et al. also fail to teach an SMBus, however, Maxim/Dallas Semiconductor teach that SMBus, and SMBus devices are essentially compatible with I2C buses and devices (page 1). Because the two elements are functionally equivalent, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to substitute an SMBus in place of an I2C bus in the system of Loh et al. This would have been obvious since Maxim/Dallas Semiconductor teaches that the SMBus offers error recovery, while the I2C bus offers none (page 2)

With regard to claim 12, Loh et al. teach an information handling system comprising a portable information handling system (paragraph 10, claim 1; where a portable information handling system may be interpreted as a portable computing device).

With regard to claim 13, Bajikar teaches a method comprising:

Communicating the external input device inputs to a second microcontroller (page 16, where it would be obvious to one of ordinary skill in this art to connect an external input device such as a mouse or keyboard to the illustrated "external ps/2 ports");

Bajkar fails to explicitly state detecting user inputs at an external input device, however since the reference does teach an external input device (see previous paragraph), it would be obvious to one of ordinary skill in the art at the time of invention by applicant to detect inputs on said device in order to process them, thereby rendering the said device useful.

Bajikar fails to disclose the details of the remaining elements of claim 13, however Bajikar et al., does provide a more detailed description of the same invention, and thus these details are inherent in the method of Bajikar. Bajikar et al. teach a method comprising:

Converting the inputs with the microcontroller into HID packets for communication to the motherboard (motherboard: paragraph 9; HID packets: paragraph 17).

Processing HID packets from the integrated pointing device and integrated keyboard as trusted packets (paragraph 16, 17);

Processing HID packets for the external input device as non-trusted packets (paragraph 19 describes preventing trusted data cycles from being exposed to external (input) devices. Examiner identifies this as being equivalent to processing external

input as non-trusted packets. Additionally, paragraph 17 teaches that keystroke and pointer data may be provided to either the trusted or untrusted interfaces).

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bajikar in view of Bajikar et al., in view of Loh et al., in view of Maxim/Dallas Semiconductor, and further in view of Mueller.

Bajikar, Bajikar et al., Loh et al., and Maxim/Dallas Semiconductor fail to teach a dual SMBus for bidirectional communication.

Mueller teaches that full-duplex transmission allows for simultaneous full bandwidth transmission in both directions along with reducing start-up and turnaround delays. It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to incorporate a dual SMBus to gain these advantages (column 1, lines 12 – 27).

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bajikar in view of Bajikar et al., in view of Loh et al., in view of Maxim/Dallas Semiconductor, and further in view of Rollig et al.

Bajikar, Bajikar et al., Loh et al., and Maxim/Dallas Semiconductor fail to teach a method where extracting the HID packets further comprises receiving the SMBus messages at a state machine associated with the motherboard, and transferring the SMBus messages having HID packets to HID registers accessible to one or more information processing systems.

Rollig et al. teach extracting the HID packets at a state machine and transferring the SMBus messages having HID packets to HID registers accessible to one or more information processing components. (paragraphs 73, 79; claim 1, 4th paragraph, where HID registers may be interpreted as any registers able to hold HID data). Rollig et al. fail to explicitly teach a motherboard, however, teach that the state machine may be integrated into a circuit chip (paragraph 73). It would have been well-known to one of ordinary skill in the art at the time of invention by applicant to affix the said circuit chip onto a motherboard in order to mount it and provide it with connectivity to a bus.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to include the method of Rollig et al. in the method of Bajikar, Bajikar et al., Loh et al., and Maxim/Dallas Semiconductor in order to provide a means of extracting the HID packets from the motherboard and transferring them to HID registers. This would have been obvious since Rollig et al. teach that a finite state machine can receive and interpret instructions and data, and transfer the data between an SMBus interface and register set (paragraph 73, 79; claim 1).

Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Loh et al. in view of Maxim/Dallas Semiconductor.

With regard to claim 16, Loh et al. teach a system for communicating trusted user inputs from a user input deice to information processing components of an information handling system, the system comprising:

A microcontroller operable to accept user inputs from an integrated keyboard and an integrated pointing device, to convert the user inputs into a format readable by processing components, and to embed the formatted user inputs into I2C-compatible messages (paragraph 10, 11, 13, 15, 20; where a keyboard controller may be interpreted as a microcontroller).

An I2C-compatible bus interfaced with the microcontroller and operable to transfer the formatted user inputs (paragraph 13, 15, 20; where a keyboard controller may be interpreted as a microcontroller). Loh et al. fail to explicitly describe a motherboard, however, examiner notes a motherboard would have been an inherent structure in the system of Loh et al. in order to provide a means of mounting and interconnecting components and buses.

A processing component interfaced with the I2C bus and operable to extract the formatted user inputs from the I2C bus messages (paragraph 15, where a main CPU may be interpreted as a processing component).

Loh et al. fail to teach an SMBus, however, Maxim/Dallas Semiconductor teach that SMBus, and SMBus devices are essentially compatible with I2C buses and devices (page 1). Because the two elements are functionally equivalent, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to substitute an SMBus in place of an I2C bus in the system of Loh et al. This would have been obvious since Maxim/Dallas Semiconductor teaches that the SMBus offers error recovery, while the I2C bus offers none (page 2)

With regard to claim 17, Loh et al. teaches the additional limitation wheren the formatted user inputs comprise HID packets (paragraph 11 describes receiving inputs from a keyboard or graphical pointing device). Loh et al. does not explicitly teach HID packets, however, examiner interprets HID packets as being any data packet produced by a human interface device, such as a keyboard. Additionally, Loh et al. does not explicitly teach formatting of the user inputs. Examiner recognizes that in order for a keyboard controller to be useful, it must have some processing capability, and therefore, formatting the inputs it receives would be inherent to its function.

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Loh et al. in view of Maxim/Dallas Semiconductor, and further in view of Rollig et al.

Loh et al. and Maxim/Dallas Semiconductor fail to teach the system of claim 17 wherein the processing component interfaced with the SMBus comprises a state machine and one or more HID registers.

Rollig et al. teach a state machine interfaced with the SMBus and one or more HID registers (paragraph 73, 79; claim 1, 4th paragraph). It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to include the state machine of Rollig et al. in the system of Loh et al. and Maxim/Dallas Semiconductor in order to provide a means of extracting the formatted user inputs from the SMBus messages. This would have been obvious since Rollig et al. teach that a finite state machine can serve as an SMBus message handler; able to receive and interpret

instructions and data and transfer the data between the SMBus interface and a register set (paragraph 73, 79).

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Loh et al. in view of Maxim/Dallas Semiconductor, in view of Rollig et al., and further in view of Mueller.

Loh et al., Maxim/Dallas Semiconductor, and Rollig et al. fail to teach a dual SMBus for bi-directional communication.

Mueller teaches that full-duplex transmission allows for simultaneous full bandwidth transmission in both directions along with reducing start-up and turnaround delays. It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to incorporate a dual SMBus to gain these advantages (column 1, lines 12 – 27).

Claims 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Loh et al. in view of Maxim/Dallas Semiconductor, and further in view of Bajikar.

Loh et al. and Maxim/Dallas Semiconductor fail to teach a second microcontroller operable to accept user inputs at an external keyboard and to provide the external keyboard inputs to the motherboard through a non-trusted communication channel.

Bajikar teaches a second microcontroller operable to accept user inputs at an external keyboard and to provide the external keyboard inputs to the motherboard through a non-trusted communication channel (page 16). Although Bajikar does not

specifically teach an external keyboard, it would have been well known to one of ordinary skill in this art at the time of invention by applicant that an external keyboard can be connected to an external PS/2 port, which the Bajikar does teach, and is connected to the second microcontroller.

Bajikar fails to disclose the remaining details of claim 20, however Bajikar et al., does provide a more detailed description of the same invention, and thus these details are inherent in the system of Bajikar. Bajikar et al. teach a system comprising:

Processing HID packets for the external input device as non-trusted packets (paragraph 19 describes preventing trusted data cycles from being exposed to external (input) devices. Examiner identifies this as being equivalent to processing external input to the motherboard through a non-trusted communication channel. Additionally, paragraph 17 teaches that keystroke data may be provided to either the trusted or untrusted interfaces).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Spittle whose telephone number is (571) 272-2467. The examiner can normally be reached on Monday - Friday, 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MDS

Khanh Dang
Primary Examiner